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EXAMINER
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BONZO, BRYCE P

ART UNIT	PAPER NUMBER
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2113

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



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**MAILED**

**JUN 12 2007**

**Technology Center 2100**

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/644,628  
Filing Date: August 19, 2003  
Appellant(s): DUNSTAN, ROBERT A.

\_\_\_\_\_  
Richard B. Leggett, Reg No. 59,485  
Schwabe, Williamson & Wyatt, P.C.  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed January 19<sup>th</sup>, 2007 appealing from the Office action mailed August 22<sup>nd</sup>, 2006.

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**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

5,838,982	Cooper et al.	11-1998
2004/0088589	Westerinen	5-2004

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### **(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has amended to the claims to define "negated" and remove "ignored" from the specification in an attempt to overcome the prior art.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen (United States Patent Publication No. 2004/0088589) in view of Cooper (United States Patent No. 5,838,982).

Westerinen discloses:

1. In an apparatus, a method of operation comprising:

receiving a state signal signaling whether the apparatus is in an AC failure state (§27 shows the use of switch over signals in a switch over circuit; §28 shows the use of initiate a failover);

receiving a power button event signal signaling an event associated with a power button of the apparatus (§21: power button event signal generated and received); and

*providing special handling if the state signal signals the apparatus is in the AC failure state (§30 describes a specialized handling if power switching is requested during a power event).*

Westerinen does not explicitly disclose:

negating the power button event signal if the state signal signals the apparatus is in the AC failure state.

Cooper discloses these features at Figure 2 the decision tree path corresponding to Blocks 106→ 108→ 110→ 112→ END. Column 3, lines 37 disclose the initiation of the this decision tree path. Column 4, lines 9-34 describe this as active code processing in a computer system, and therefore an active decision making process.

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

As per claim 2-5, Westerinen discloses:

2. The method of claim 1, wherein the method further comprises

monitoring for absence of AC to a power supply of the apparatus (§26: a switchover circuit monitor for power failure); and

generating a power signal signaling AC failure on detection of absence of AC to the power supply. (§27: signal generated by the switch over circuit)

3. The method of claim 2, wherein the monitoring and generating are performed by the power supply (Figure 3, item 76 switchover circuit within power supply).

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4. The method of claim 2, wherein the method further comprises a selected one of outputting the power signal as the state signal, and forming the state signal based at least in part on the power signal (§33: outputting signal indicates the power state of the system).

5. The method of claim 1, wherein the event associated with a power button of the apparatus comprises a power button being pressed event (§21: event signal is generated when the button is pressed).

As per claim 6, Cooper discloses:

6. The method of claim 1, wherein the negating comprises combining the state signal and the power button event signal (Figure 2,item 112 and column 3, lines 33-65 the power event button is ignored if the system does not have available power)

As per claim 7, Westerinen discloses:

7. The method of claim 1, wherein the method further comprises  
receiving a device wake event signal signaling a device wake event of the apparatus (§21: event signal generated when button is depressed);

As per claim 7, Cooper discloses:

negating the device wake event signal, if the state signal signals the apparatus is in the AC failure state (Figure 2,item 112 and column 3, lines 33-65 the power event button is ignored if the system does not have available power).

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Cooper discloses:

negating the device wake event signal, if the state signal signals the apparatus is in the AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

As per claim 8, Westerinen discloses:

In an apparatus, a method of operation comprising:

receiving a state signal signaling whether the apparatus is in an AC failure state [para 0027: signals generated by, switchover circuit];

receiving a device wake event signal signaling a device wake event of the apparatus [para 0021 : power button event signal generated and received]; and  
*negating the device wake event signal if the state signal signals the apparatus is in the AC failure state.*

Westerinen does not disclose:

negating the device wake event signal if the state signal signals the apparatus is in the AC failure state.

Cooper discloses:

negating the device wake event signal if the state signal signals the apparatus is



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in the AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

9. The method of claim 8, wherein the method further comprises

monitoring for absence of AC to a power supply of the apparatus (¶26: switchover circuit monitor for power failure); and  
generating a power signal signaling AC failure on detection of absence of AC to the power supply (¶27: signals generated by switchover circuit).

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10. The method of claim 9, wherein the monitoring and generating are performed by the power supply (Figure 3, reference 76: switchover circuit within power supply).

11. The method of claim 9, wherein the method further comprises a selected one of outputting the power signal as the state signal, and forming the state signal based at least in part on the power signal (§33: outputting signal indicate the power state).

As per claim 12, Westerinen discloses:

The method of claim 8, wherein the negating comprises combining the state signal [para 0033: power state signal] and the device wake event signal [para 0021: power button signal].

Westerinen does not disclose:

The method of claim 8, wherein the negating comprises combining the state signal and the device wake event signal.

Cooper discloses:

wherein the negating comprises combining [Figure 2, reference 112 and column 3, lines 33-65: power button event signal is ignore (negating) if system does not have available power source (AC failure state)] the state signal and the power button event signal.

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

As per claim 13, Westerinen discloses:

13. A system comprising:

an arrangement to generate a state signal signaling whether the system is in an AC failure state [para 0027 and Figure 3: arrangement to generate a state signal];  
and

a first circuit coupled [Figure 3, reference 36: controller] to the arrangement to receive the state signal and a power button event signal indicating an event associated with a power button of the system [para 0021 and para 0033: power

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button event signal and state signal received by controller], and

Westerinen does not disclose:

to negate the power button event signal if the state signal signals the AC failure state.

Cooper discloses:

to negate the power button event signal if the state signal signals the AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

14. The system of claim 13, wherein the system further comprises a monitor to monitor for presence or absence of AC to a power supply of the system (§26: switchover circuit monitor for power failure), and to generate a power signal signaling accordingly. (§27: signals generated by switchover circuit)

15. The system of claim 14, wherein the system further comprises the power supply, and the monitor is an integral part of the power supply (Figure 3, reference 76: switchover within power supply).

16. The system of claim 14, wherein the system further comprises a second circuit (Figure 3: switch over circuit) coupled to the power supply and the first circuit, to generate the state signal based at least in part on the power signal, and to provide the first circuit with the state signal (29: generate signal to indicate state).

17. The system of claim 13, wherein the first circuit comprises a signal combiner circuit element to combine the state signal and the power button event signal (figure 3, reference 36, 86 and 50: state and power button event signal combined in controller, signal circuit is therefore inherent).

As per claim 18, Westerinen discloses:

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The system of claim 13, wherein the system further comprises at least one hardware element equipped to generate a device wake event signal signaling a device wake event of the system (§29); and

Westerinen does not disclose:

the first circuit is also equipped to negate the device wake event signal, if the state signal signals the apparatus is in the A C failure state.

Cooper discloses:

the first circuit is also equipped to negate the device wake event signal, if the state signal signals the apparatus is in the AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

19. The system of claim 13, wherein the system further comprise a networking interface (§21: LAN and modem communication can trigger a wake up event (networking interface is inherent).)

As per claim 20, Westerinen discloses:

A system comprising:

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an arrangement to generate a state signal signaling whether the system is in an AC failure state [para 0027 and Figure3: arrangement to generate a state signal]; and

a first circuit coupled [Figure 3, reference 36: controller] to the arrangement to receive the state signal and a device wake event signal signaling a device wake event of the system [para 0021 and para 0033: power button event signal and state signal received by controller], and

to negate the device wake event signal if the state signal signals the AC failure state.

Westerinen does not disclose:

to negate the power button event signal if the state signal signals the AC failure state.

Cooper discloses:

to negate the power button event signal if the state signal signals the AC failure state [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a

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power failure state is well known in the art and power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

21. The system of claim 20, wherein the system further comprises a monitor to monitor for presence or absence of AC to a power supply of the system (§26), and to generate a power signal signaling accordingly (§27)

22. The system of claim 21, wherein the system further comprises the power supply, and the monitor is an integral part of the power supply (Figure 3, reference 76: switchover circuit within power supply).

23. The system of claim 21, wherein the system further comprises a second circuit (Figure 3, reference 86: switch over circuit) coupled to the power supply and the first circuit, to generate the state signal based at least in part on the power signal, and to provide the first circuit with the state signal (§29: generate signal to indicate state).

24. The system of claim 20, wherein the first circuit comprises a signal combiner



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circuit element to combine the state signal and the device wake event signal

(Figure 3, items 36, 86 and 50)

25. The system of claim 20, wherein the system further comprise a networking interface (¶21).

As per claim 26, Westerinen discloses:

An apparatus comprising:

a first input terminal [Figure 3, reference 86 to 36: input terminals to the controller] to receive a first signal indicating presence or absence of AC to a power supply of a system [para 0027: signals generated by switchover circuit to the controller];

a second input terminal to receive a second signal indicating a power button event of the system apparatus [Figure 3, reference 50: power button event signal across a second input terminal on a controller]; and

a first combiner circuit element coupled to the first and second input terminals to combine the two signals [Figure 3, references 36, 38, and 50: state signal and power button event signal combined in controller, signal combiner circuit inherent] to negate the second signal whenever the first signal signals absence of AC to the power supply.

Westerinen does not disclose:

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to negate the second signal whenever the first signal signals absence of AC to the power supply.

Cooper discloses:

to negate the second signal whenever the first signal signals absence of AC to the power supply [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and is power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

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As per claim 27, Westerinen discloses:

The apparatus of claim 26, wherein the apparatus further comprises

a third input terminal to receive a third signal indicating a device wake event of the system [Figure 3, reference 26 and para 0029: battery driver supplies a wake signal to the controller through a third input terminal]; and a second combiner circuit element coupled to the first and third input terminals to combine the two signals [Figure 3, references 36, 26, and 50: state signal and power button event signal combined in controller, signal combiner circuit inherent] to negate the third signal whenever the first signal signals absence of AC to the power supply.

Westerinen does not disclose:

negate the third signal whenever the first signal signals absence of AC to the power supply.

Cooper discloses:

negate the third signal whenever the first signal signals absence of AC to the power supply [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)]

As per claim 28, Westerinen discloses:

The apparatus of claim 27, wherein the first and third terminals are one of the

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same terminal [Figure 3, references 36: controller (a terminal in general) functions as both the first and third terminals (one of the same)] and the first and second signal combiner circuit elements are one of the same signal combiner circuit element [Figure 3, references 36: controller (combiner circuit) can perform both functions of the first and second circuits (one of the same)].

As per claim 29, Westerinen discloses: An apparatus comprising: a first input terminal [Figure 3, reference 86 to 36: input terminals to the controller] to receive a first signal indicating presence or absence of AC to a power supply of a system [para 0027: signals generated by switchover circuit to the controller];

a second input terminal to receive a second signal indicating a device wake event of the system [Figure 3, reference 50: power button event signal (device wake event) across a second input terminal on a controller]; and

a first combiner circuit element coupled to the first and second input terminals to combine the two signals [Figure 3, references 36, 38, and 50: state signal and power button event signal combined in controller, signal combiner circuit inherent] to negate the second signal whenever the first signal signals absence of AC to the power supply.

Westerinen does not disclose:

to negate the second signal whenever the first signal signals absence of AC to the power supply.

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Cooper discloses:

to negate the second signal whenever the first signal signals absence of AC to the power supply [Figure 2, reference 112 and column 3, lines 33-65: power button event signal ignore if system does not have available power source (AC failure state)].

Both Westerinen and Cooper disclose power systems. Westerinen does not disclose negating the power button signal if the system is in an AC failure state, however Cooper does. Cooper discloses a system that determines if the system has available power before powering up and if there is no power, the system ignores (negates) the power on signal. Negating the power on signal while in a power failure state is well known in the art and is power efficient. Westerinen does explicitly disclose concern about draining the battery power (power efficiency) [para 0030: mechanism to only power up the system when there is a steady power supply]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to negate the power button event signal when the system is in a power failure state as taught in Cooper into the system of Westerinen to create a more power efficient system.

As per claim 30, Westerinen discloses:

The apparatus of claim 29, wherein the first and second input terminals are input pins [Figure 3, reference 36: input terminals are pins].

### **(10) Response to Arguments**

Applicant has argued the validity of the Examiner's rejections under 35 USC §112, first paragraph regarding the use of "negating" in the claims and its subsequent manipulation in the specification (page 15, prior to amending).

First, Applicant forms the association of negate = suppress OR ignore (page 15, lines 1-14). This is done by the first sentence establishing the use of negating, while the second sentence describes two manner of negating, those being suppressing OR ignoring a wake event. These terms have do not have a clear and distinct meaning in common usage or in the technical arts, and the Examiner was required while interpreting the prior art over the claimed limitations in claim 1 to delve into the specification for guidance.

Following the application of prior art which discloses the claimed invention under 35 USC §102 (the practice of ignoring a wake signal) Applicant clearly, breaks the "negate=suppress OR ignore" definition relied upon during the initial examination by amendment to the specification rather than the claims. It is the view of the Examiner, this constitutes addition by deletion, a valid rational for a rejection under 35 USC §112.

Applicant has effectively invented the claimed invention during the prosecution by amending the specification, rather than amending the claims to overcome the prior art. It is believed that Applicant had hoped to force the Examiner to provide a second action Non-Final on the unamended claim, by changing the scope of specification and this change trickling back into the claim.

Second, Applicant argues the combination of Westerinen and Cooper is deficient. Applicant argues Cooper does not disclose the negating of a power signal. The Examiner points to figure 3, item chain 106→ 108→ 110→ 112→ END. This is as described in the specification at column 4, a clear and deliberate program which has positive steps and decisions and must be performed by a powered computer.

Cooper is relevant, contrary to Applicant's assertions, because the system is clearly operating while these decisions are being made. Column 4, is the operating pseudo code of a the computer, deliberately parsing a decision tree, and is not as Applicant assert an unpowered computer not performing actions.

Further, Applicant never claims the nature as to when or why the power button is activated is not claimed. Additionally, Cooper is clearly describing a relevant and related power architectures, as Cooper is the same assignee (INTEL) in the same environment as the present invention.

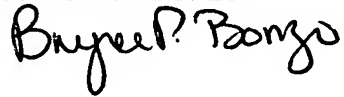
Further, Applicant argues there is no reason to combine Cooper and Westerinen. The Examiner points out, the references do commonly disclose power conservation mechanisms which are compatible and together provide a clear advantage over the prior art. Both references deliberately point out they are open to modification and are not to be used in a vacuum.

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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Bryce Patrick Bonzo

A handwritten signature in black ink that reads "Bryce P. Bonzo". The signature is written in a cursive, slightly stylized font.

Conferees:

Robert Beausoliel

A handwritten signature in black ink that reads "R. Beausoliel". The signature is written in a cursive, slightly stylized font.

Scott Baderman

A handwritten signature in black ink that reads "S. Baderman". The signature is written in a cursive, slightly stylized font.